SONY

ILX523A

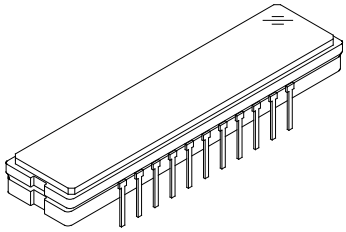
2700 pixel CCD Linear Sensor (B/W)

Description

The ILX523A is a reduction type CCD linear sensor designed for facsimile, scanner and OCR use. This sensor reads A3 size documents at a density of 200 DPI (Dot Per Inch).

In addition, this can be directly driven at 5V logic and operate on single 12V power supply for easy use.

22 pin DIP (Cer-DIP)



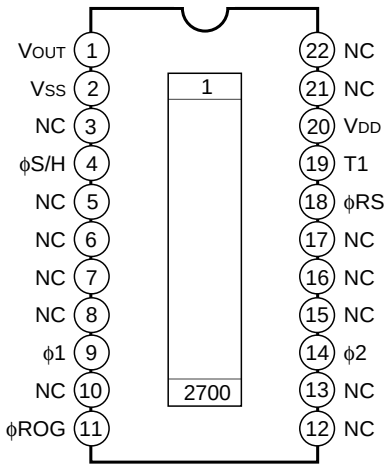
Features

- Number of effective pixels: 2700 pixels
- Pixel size: 11µm × 11µm (11µm pitch)
- Ultra low lag/High Sensitivity
- Built-in Feed through suppression circuit
- Built-in Sample-and-hold circuit
- Maximum data rate: 5MHz
- Single 12V power supply

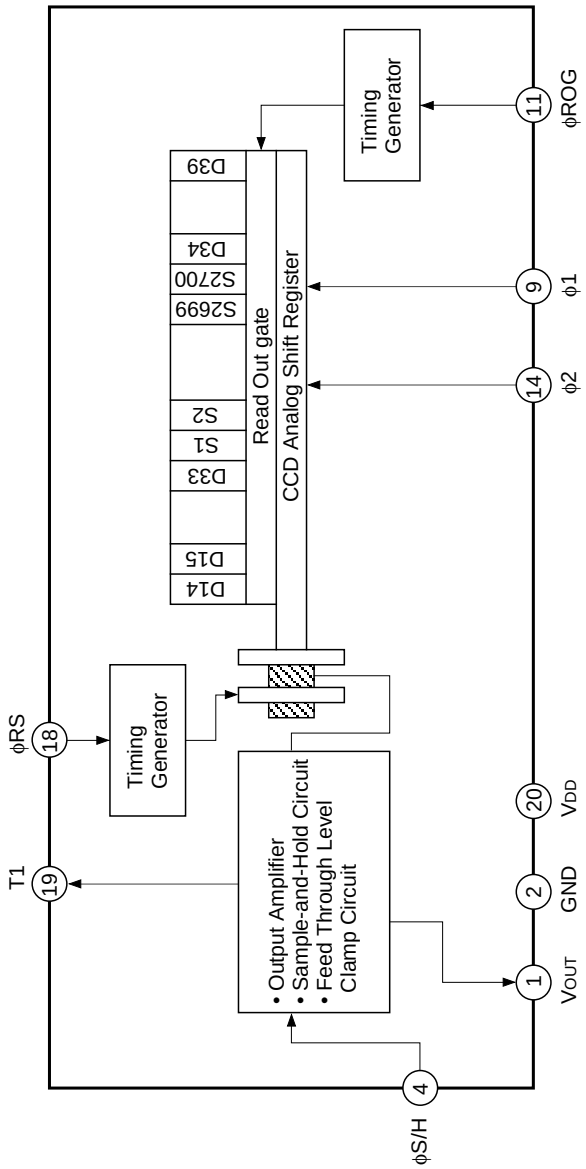
Absolute Maximum Ratings

• Supply voltage	V_{DD}	15	V
• Operating temperature		–10 to +60	°C
• Storage temperature		–30 to +80	°C

Pin Configuration (Top View)



Block Diagram



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Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	V_{OUT}	Signal output	12	NC	NC
2	GND	GND	13	NC	NC
3	NC	NC	14	ϕ2	Transfer pulse 2
4	ϕS/H	Sample-and-Hold pulse	15	NC	NC
5	NC	NC	16	NC	NC
6	NC	NC	17	NC	NC
7	NC	NC	18	ϕRS	Reset gate pulse
8	NC	NC	19	T1	Test pin (Open)
9	ϕ1	Transfer pulse 1	20	V_{DD}	12V power supply
10	NC	NC	21	NC	NC
11	ϕROG	Read out gate pulse	22	NC	NC

Note) Connect Pin 4 to GND when not using internal sample-and-hold circuit.

Recommended Pin Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD}	11.4	12.0	12.6	V

Clock Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacitance of ϕ1	$C_{\phi 1}$	—	300	—	pF
Input capacitance of ϕ2	$C_{\phi 2}$	—	300	—	pF
Input capacitance of ϕROG	$C_{\phi ROG}$	—	10	—	pF
Input capacitance of ϕRS	$C_{\phi RS}$	—	10	—	pF
Input capacitance of ϕS/H	$C_{\phi S/H}$	—	10	—	pF
Data Rate	—	—	1.0	5.0	MHz

Electrooptical Characteristics

(Ta = 25°C, V_{DD} = 12V, data rate = 1MHz, mode without S/H (Pin 4 = GND), light source = 3200K, IR cut filter CM-500S (t = 1.0mm) used)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity	R1	66.5	95	123.5	V/(lx · s)	Note 1
Sencitivity nonuniformity	PRNU	—	2.0	10.0	%	Note 2
Saturation output voltage	V_{SAT}	2.0	2.5	—	V	—
Dark voltage average	V_{DRK}	—	2.0	8.0	mV	Note 3
Dark signal nonuniformity	DSNU	—	7.0	14.0	mV	Note 3
Image Lag	IL	—	0.02	—	%	Note 4
Dynamic range	DR	—	1250	—	—	Note 5
Saturation exposure	SE	—	0.02	—	lx · s	Note 6
Supply current	I_{VDD}	—	15.0	25.0	mA	—
Total transfer efficiency	TTE	92.0	98.0	—	%	—
Output impedance	Z_O	—	300	—	Ω	—
Offset level	V_{OS}	—	7.4	—	V	Note 7

Notes)

1. For the sensitivity test, light is applied with a uniform intensity of illumination.
2. PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 1. The output signal amplitude for test is 1V.

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

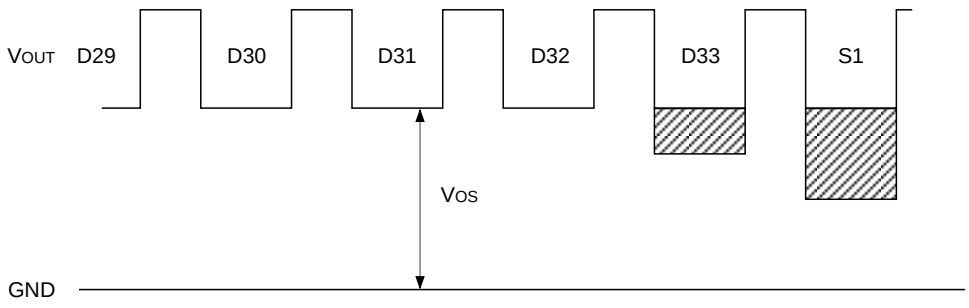
   The maximum output of all the valid pixels is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.
3. Optical signal accumulated time stands at 10ms.
4. Output signal amplitude V_{OUT} = 500mV.
5. Dynamic range is defined as follows.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

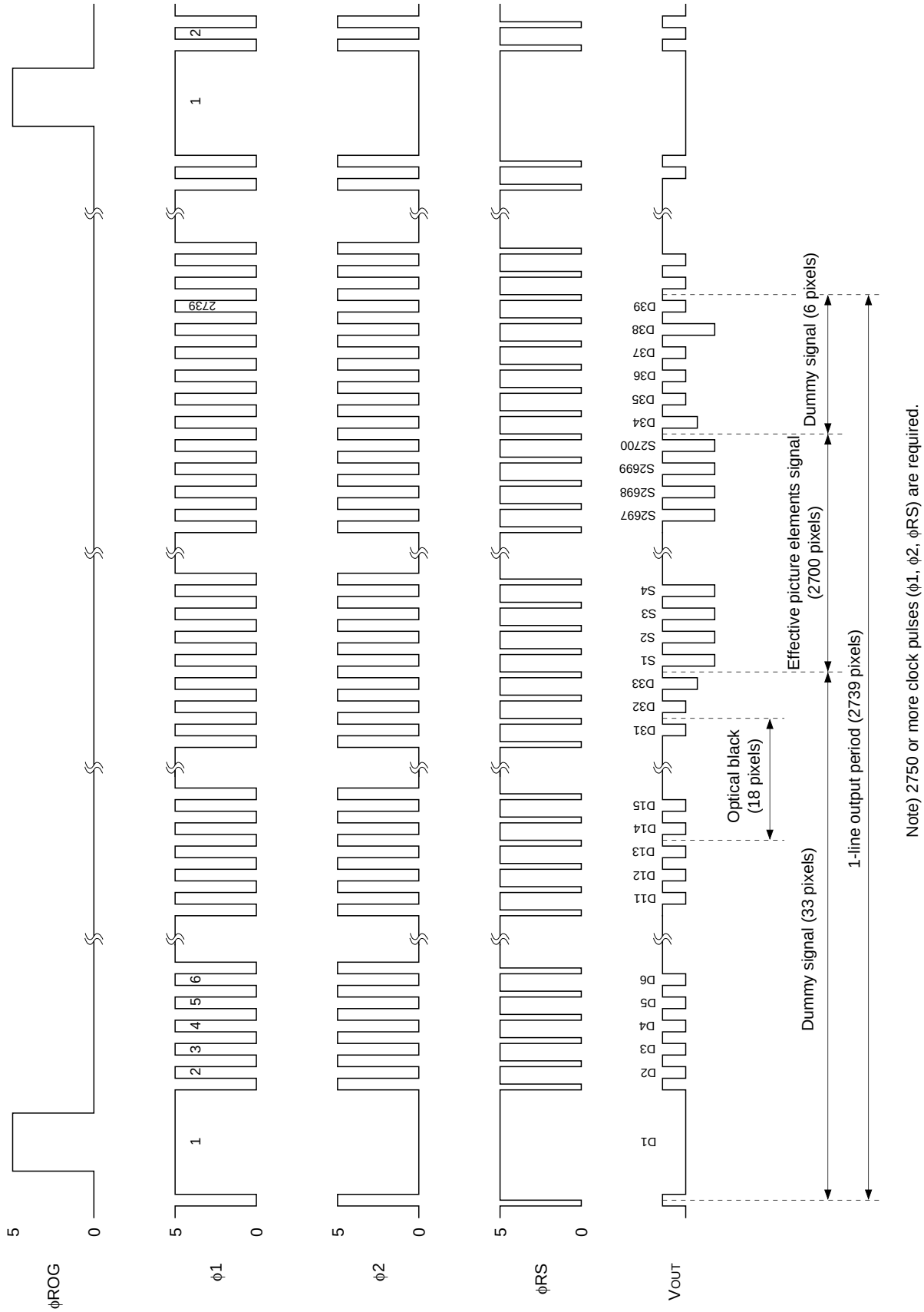
   When the optical signal accumulated time is shorter, the dynamic range gets wider because the optical signal accumulated time is in proportion to the dark voltage.
6. Saturation exposure is defined as follows.

$$SE = \frac{V_{SAT}}{R1}$$

7. V_{OS} is defined as indicated below.

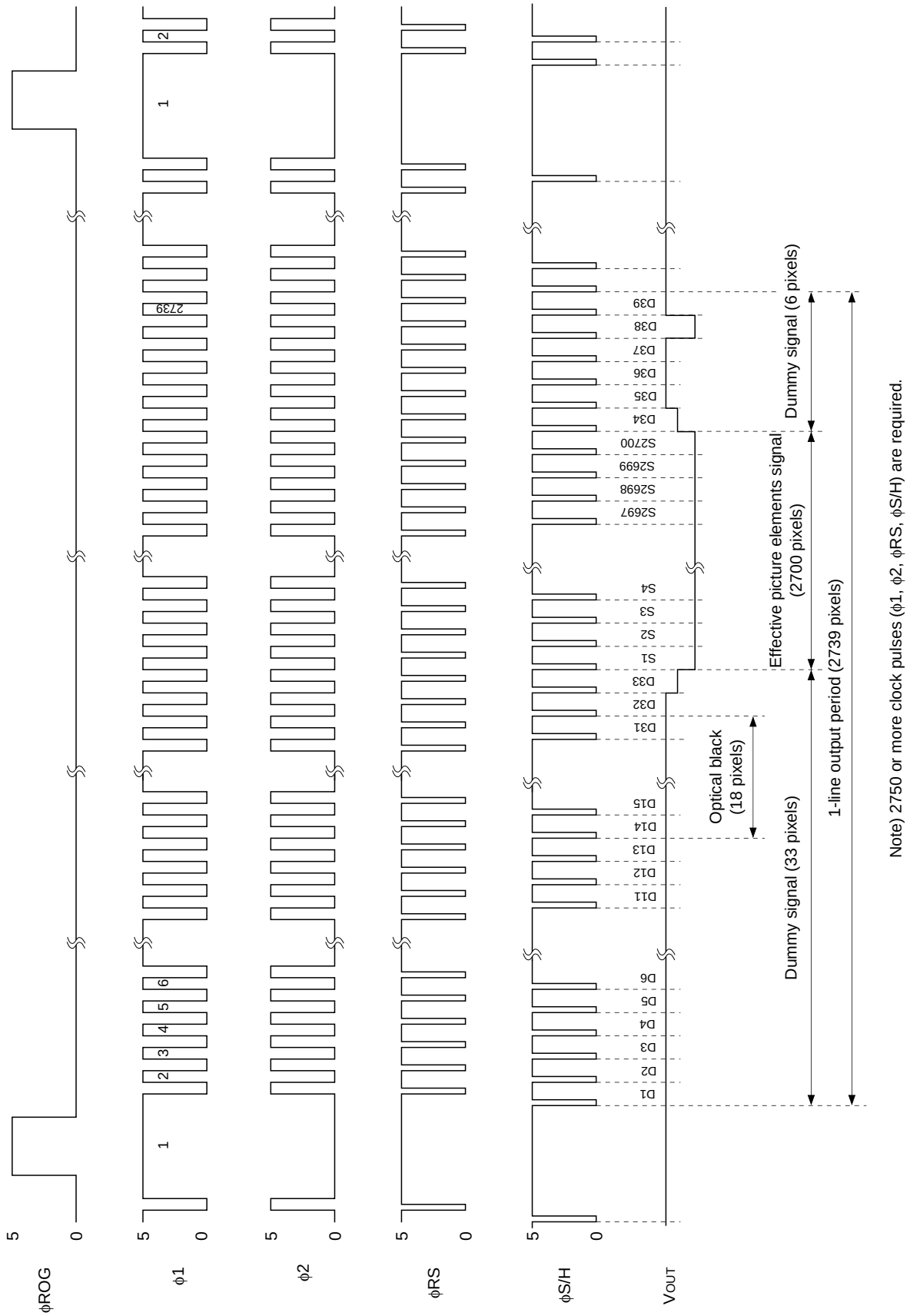


Clock Timing Diagram (without internal sample-and-hold circuit)



Note) 2750 or more clock pulses (φ1, φ2, φRS) are required.

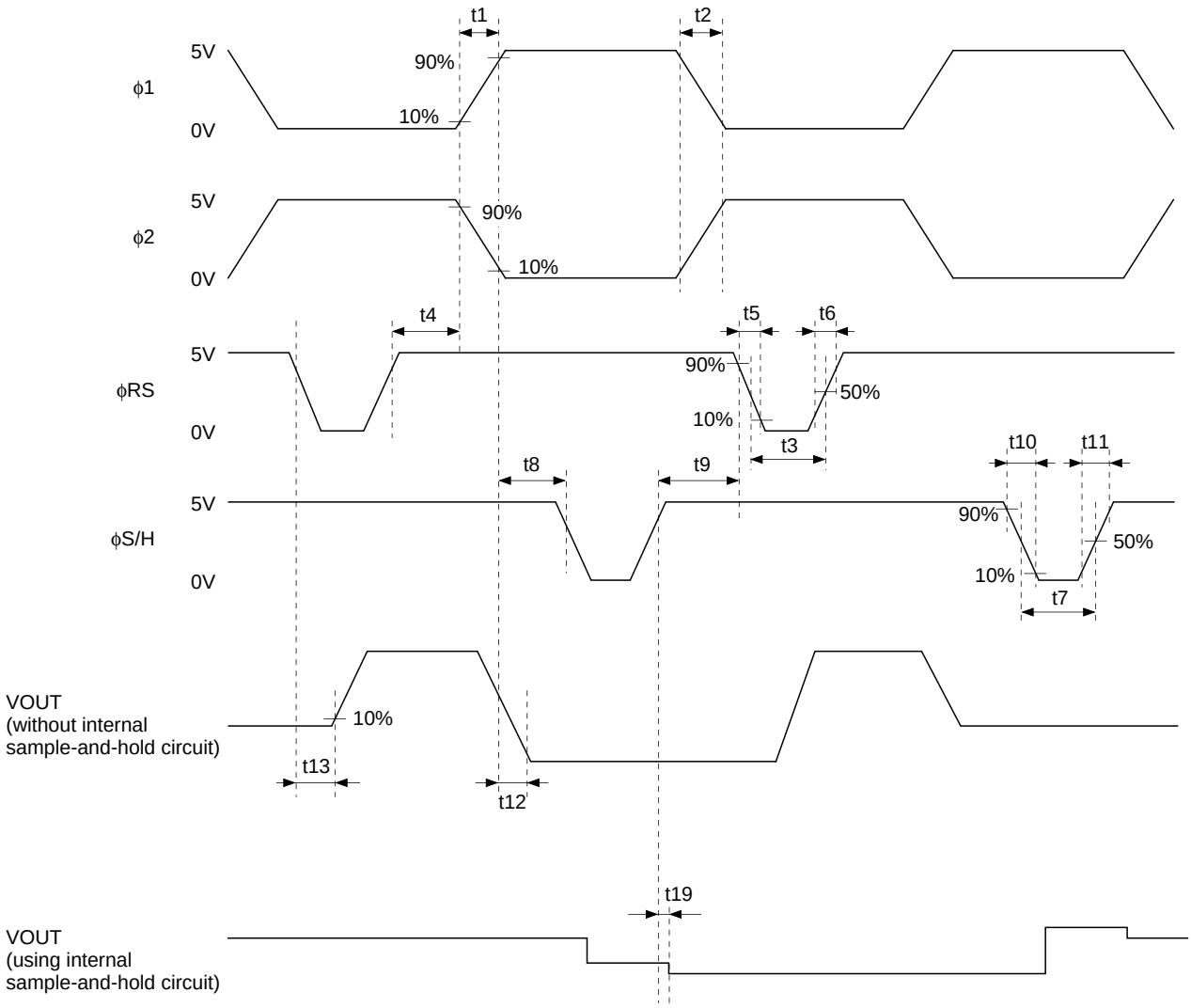
Clock Timing Diagram (using internal sample-and-hold circuit)



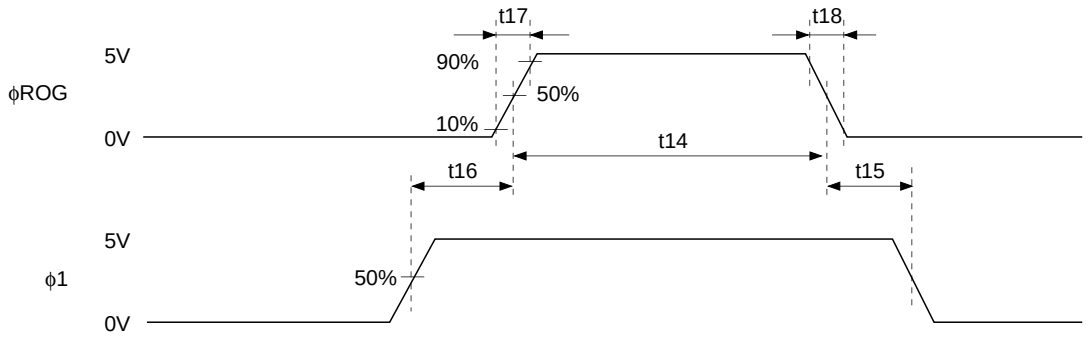
Note) 2750 or more clock pulses (φ1, φ2, φRS, φS/H) are required.

Input Clock Waveform Conditions

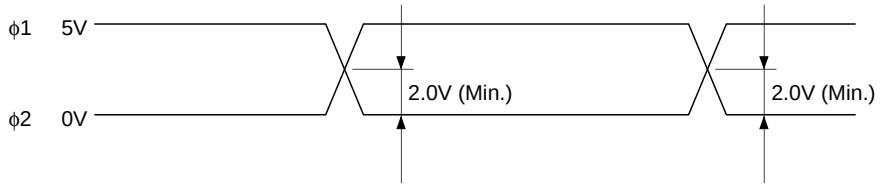
φ1, φ2, φRS, φS/H pulses related



φROG, φ1 pulses related



Cross point ϕ1 and ϕ2

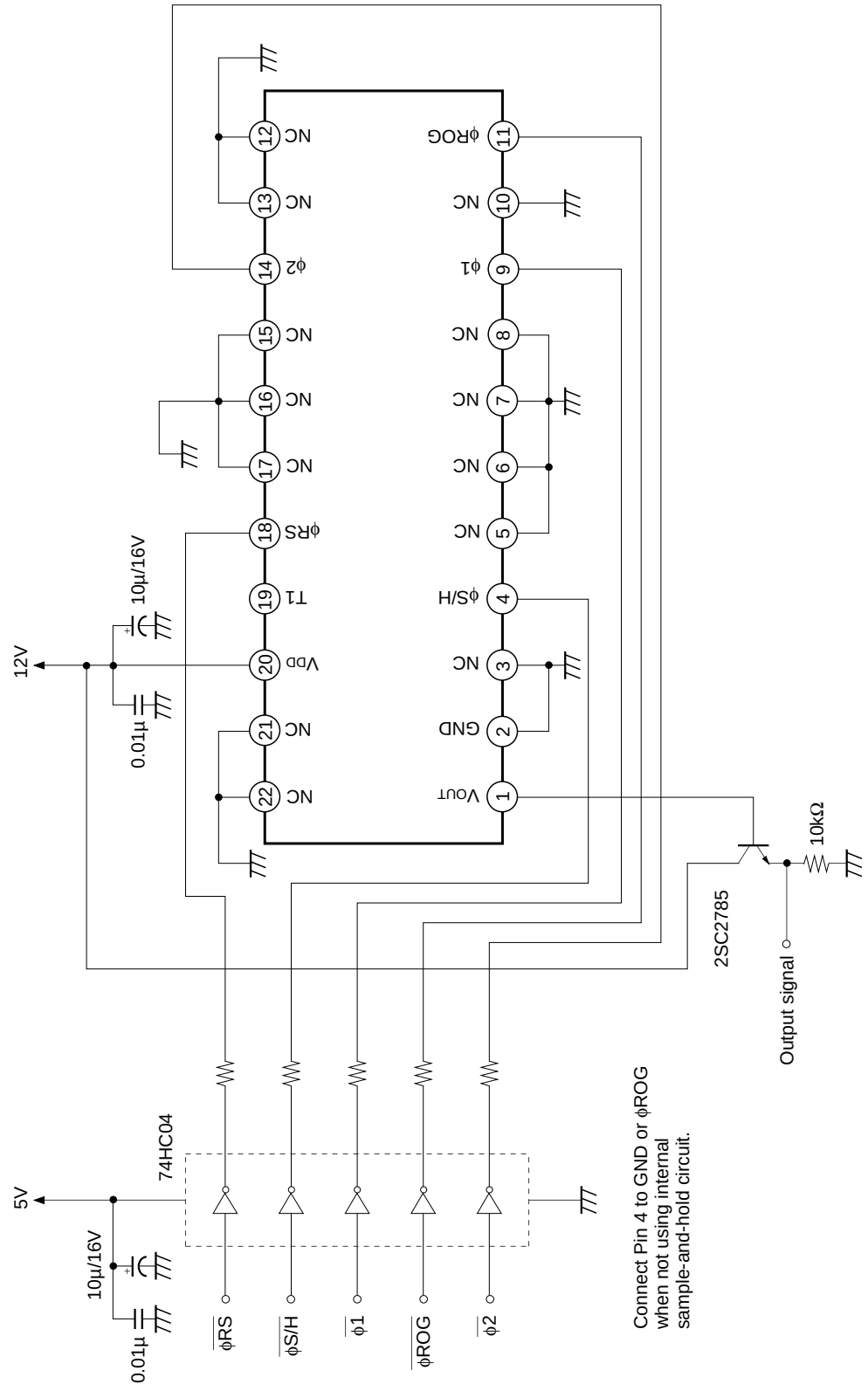


Input Clock Waveform Conditions

Item		Symbol	Min.	Typ.	Max.	Unit
ϕ1, ϕ2 rise/fall time		t1, t2	0	50	100	ns
ϕRS pulse low level period		t3	20	80*1	200	ns
ϕ1, ϕ2 – ϕRS pulse timing		t4	25	200*1	350	ns
ϕRS rise/fall time		t5, t6	0	10	40	ns
ϕS/H pulse low level period		t7	20	80*1	200	ns
ϕ1, ϕ2 – ϕS/H pulse timing		t8	70	200*1	350	ns
ϕRS – ϕS/H pulse timing		t9	15	—	—	ns
ϕS/H rise/fall time		t10, t11	0	10	40	ns
Signal output delay time		t12	—	40	—	ns
		t13	—	20	—	ns
		t19	—	20	—	ns
ϕROG pulse high level period		t14	500	1000	—	ns
ϕ1 – ϕROG pulse timing		t15, t16	500	1000	—	ns
ϕROG rise/fall time		t17, t18	0	50	100	ns
Inpuyt clock pulse voltage	High level		4.5	5	5.5	V
	Low level		0	—	0.5	V

*1 Recommended conditions for data rate = 1MHz.

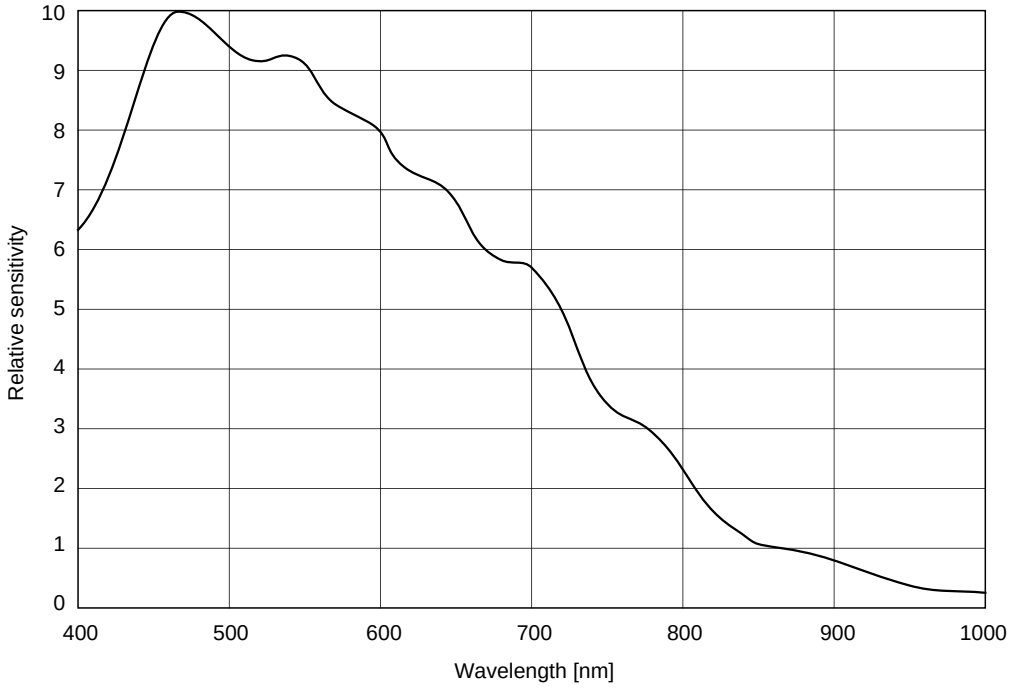
Application Circuit



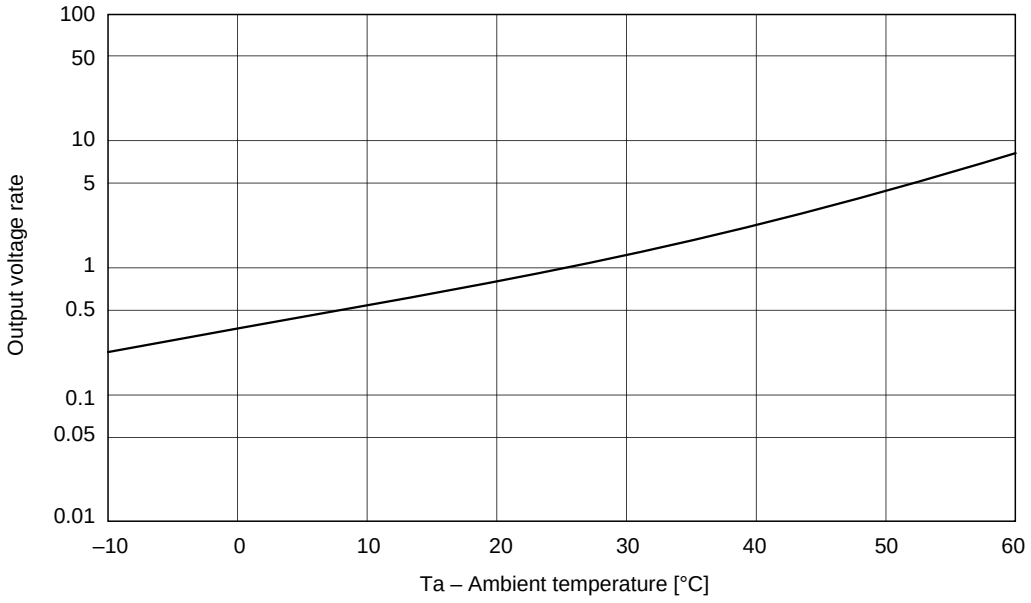
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (V_{DD} = 12V, Ta = 25°C)

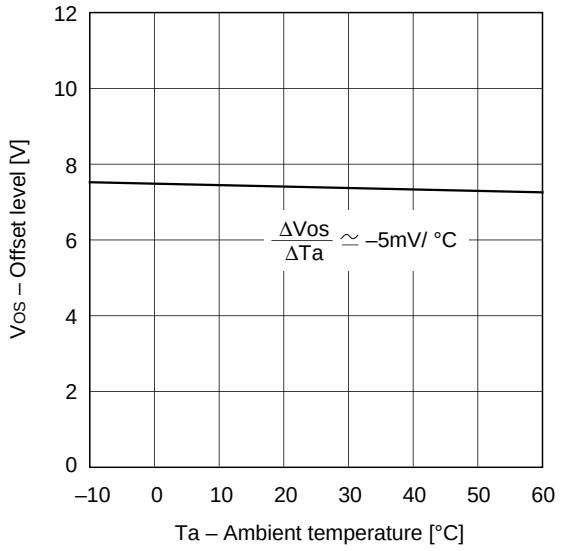
Spectral sensitivity characteristics (Standard characteristics)



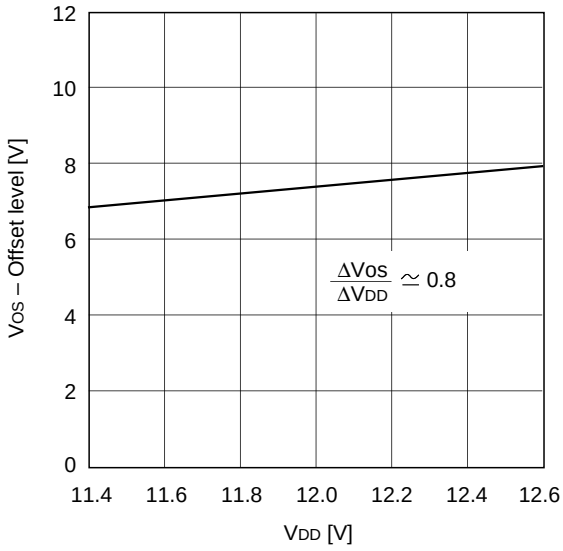
Dark signal output temperature characteristics (standard characteristics)



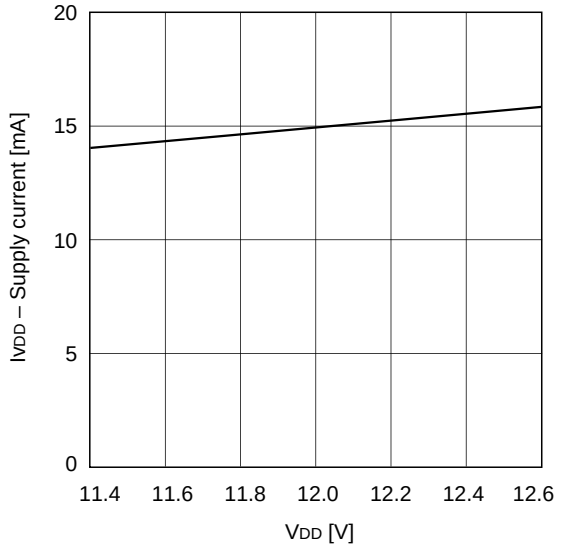
Offset level vs. Temperature characteristics (Standard characteristics)



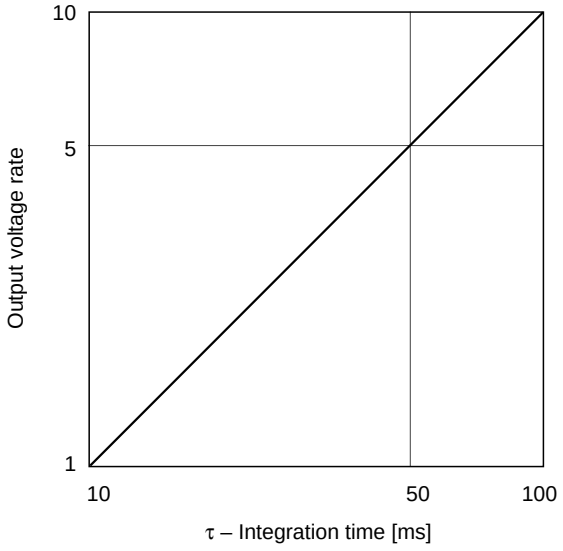
Offset level vs. V_{DD} characteristics (Standard characteristics)



Supply current vs. V_{DD} characteristics (Standard characteristics)



Output voltage vs. Integration time (Standard characteristics)



Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non chargeable gloves, clothes or material.
Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensor.

e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Cer-DIP Packages

The following points should be observed when handling and installing Cer-DIP packages.

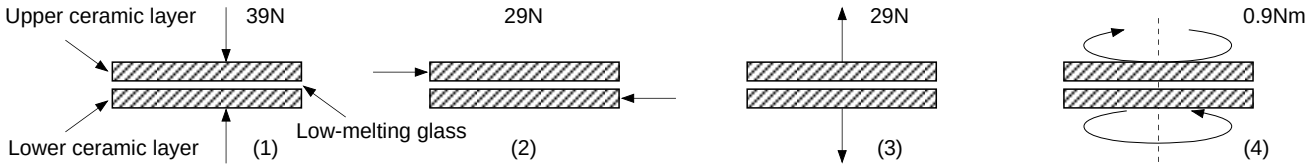
a) Remain within the following limits when applying static load to the ceramic portion of the package:

(1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)

(2) Shearing strength: 29N/surface

(3) Tensile strength: 29N/surface

(4) Torsional strength: 0.9Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.

c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,

(1) Applying repetitive bending stress to the external leads.

(2) Applying heat to the external leads for an extended period of time with soldering iron.

(3) Rapid cooling or heating.

(4) Rapid cooling or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.

(5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3) Soldering

a) Make sure the package temperature does not exceed 80°C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

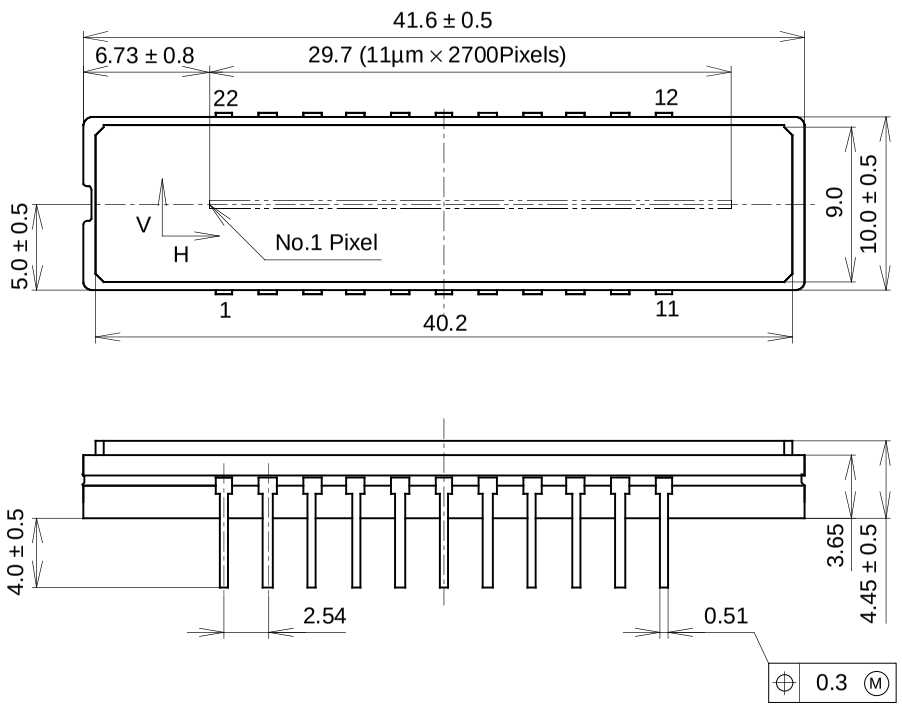
5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

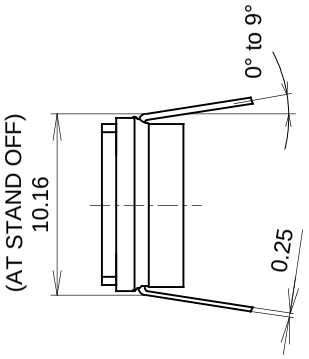
6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

7) Normal output signal is not obtained immediately after device switch on.

Package Outline Unit: mm

22pin DIP (400mil)





1. The height from the bottom to the sensor surface is 2.45 ± 0.3mm.
2. The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.2g